#2018UIC3116 #ASSIGNMENT:02

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QUE:01 With the help of suitable diagram explain the tri-state logic of TTl logic family.

ANS: Three-state logic is a logic used in electronic circuits wherein a third state, the high-impedance state, is added to the original 1 and 0 logic states that a port can be in. This high-impedance state effectively removes the port from the circuit, as if it were not part of it. So in the third state of high impedance, the output from the port is neither 1 nor 0, but rather the port does not appear to exist.

Three-state logic is also known as tri-state logic.

TTL(Transistor- transistor logic) is one of the pooular saturated logic families. Transistor is basic element of logic family which operates either in cut off saturation region.

A normal digital circuit has two output states: low and high. The output is either in high state or low state.If the output is not in low state.it is definetly in the high state. The tri state TTL has three output states :high ,low and high impendance.

In TTL with tolem pole output,Q4 is ON when the output is low and is Q3 ON when the output is high . In high impedance state, both Q4 and Q3 in the totem pole arrangement are tured OFF and as a result, the output is open or floating.

When the output is LOW , the the driver gate sinks the load current as shoen in figure. When the output is high the driver gate supplies the current to the load.

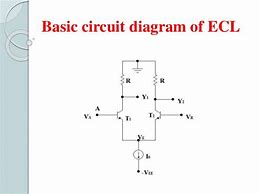
\begin{figure}
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Tri state outputs may be used with bipolar or CMOS transistors independant of logic family or logic levels. They are very usefull for buses, one active output controls the bus state (high or low) and all other outputs on the bus are passive high resistance in the third state. It should be avoided that two outputs are active at the same time, one low and the other high. A high current is flowing between these two active outputs and may destroy the outputs by excess heat.

QUE:02 Explain with help of circuit diagram the operation of a emitter coupled logic (ECL) 3 input OR/NOR gate. Show that the transistors in this circuit operate in the active region and not in saturation. Calcute the noise margins. Find the average power dissipated by the gate.Assume a base emitter voltage of 0.7 v for a transistor conducting in active region.

ANS: Emitter-coupled logic (ECL) is a high-speed integrated circuit bipolar transistor logic family. ECL uses an overdriven BJT differential amplifier with single-ended input and limited emitter current to avoid the saturated (fully on) region of operation and its slow turn-off behavior.As the current is steered between two legs of an emitter-coupled pair, ECL is sometimes called current-steering logic (CSL),current-mode logic (CML) or current-switch emitter-follower (CSEF) logic.

The circuit consists of a differential amplifier. a temperature- and voltage-compensated bias network. And an emitter-follower output. The emitter outputs require a pull-down resistor for current to flow. This is obtained from the input resistor Rp of another similar gate or from an ex tern al resistor connected to a negative voltage supply.

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In ECL, the transistors are never in saturation, the input/output voltages have a small swing (0.8 V), the input impedance is high and the output impedance is low. As a result, the transistors change states quickly, gate delays are low, and the fanout capability is high. In addition, the essentially constant current draw of the differential amplifiers minimises delays and glitches due to supply-line inductance and capacitance, and the complementary outputs decrease the propagation time of the whole circuit by reducing inverter count.

**Noise Margin Calculation**  
Logic Noise Margin is the difference between what the driver IC outputs as a valid logic voltage and what the receiver IC expects to see as a valid logic voltage. There are two different types of noise margin, one for a logic high value and one for a logic low value . For a valid logic high, the worst case noise margin for the circuit is the minimum high level voltage which may be output from the driver, minus, the minimum high level voltage which may be seen at the receiver IC. For a valid logic low, the worst case noise margin for the circuit is the maximum low level voltage which may be output from the driver; minus, the maximum low level voltage which may be seen at the receiver IC. The equations for noise margins are provided below, use the minimum of maximum numbers as described above.  
   
Noise Margin Output high = VOH [driving device] - VIH [receiving device]  
Noise Margin Output low = VIL [receiving device] - VOL [driving device]  
The higher the numbers the better, with negative numbers indicating in-operability [no Noise Margin].  
Use Minimum numbers for output High, and maximum numbers for Output Low to calculate Noise Margin.

FOR ECL

Prop. Delay= 1.45ns

Rise/fall time= o.35ns

VIH min  = -1.165v

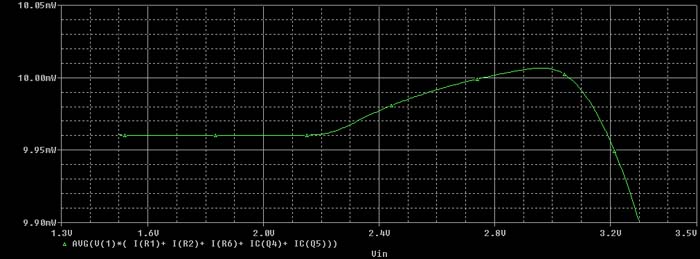
VIL max= -1.475v

VOH min = -1.025v

Vol **m**ax = -1.610v

NOISE MARGIN = 0.135V

POWER DISSIPATION :



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